rejected. With this Amendment, claims 1-2, 4-6, 11, 13, and 15 are amended, and claims 50-58 are added. Accordingly, claims 1-18 and 50-58 are at issue in the above-identified application.

I. <u>35 U.S.C. § 112(2) Indefiniteness Rejection of Claims</u>

The Examiner rejected claims 7, 9, & 11 under 35 U.S.C. § 112, second paragraph, as being indefinite. In particular, the Examiner stated that the term "a process minimum" is unclear. Applicant respectfully traverses this rejection.

Applicants disclose and use the term a "process minimum" in the specification in accordance with its ordinary meaning as known to one skilled in the art. (See Application at pg. 7 lines 4-18). A process minimum as known to one skilled in the art is the minimum dimension or line width of a component part (e.g., gate length of a transistor) permitted by the process flow design rules for building a particular semiconductor circuit. Applicants have disclosed that construction of a conventional NMOS FET utilize fabrication methods using sub-micron technology (e.g., 0.35 micron as a process minimum for a FET component dimension), which results in the NMOS FET being susceptible to junction leakage. (See Application at pg. 2 lines 18-20). As an example, Applicants disclose that the process minimum for the length of a transistor gate following a conventional 3.3 volt logic process or design rules is approximately 0.35 microns. Applicants also teach that a transistor have a recommended gate length of at least 0.4 microns (which is approximately 20% greater than the process minimum of 0.35 microns) to avoid exaggerated short channel effects associated with the conventional transistor constructed to have a gate length equal to the process minimum. In several disclosed embodiments, Applicants

also teach that the gate length be up to twice the process minimum, such as twice the minimum of 0.35 microns. (See Application at pg. 7 lines 7-18). The specification has been amended in accordance with claims 9 and 10 to further point out the subject matter which Applicants regard as an aspect of the invention. No new matter has been added by this amendment.

Thus, Applicants submit that the term "process minimum" is clearly defined and supported by the specification, and request that this rejection be withdrawn.

V. 35 U.S.C. § 103(a) Obviousness Rejection of Claims

Claims 1-6, 8, and 17-18 were rejected under 35 U.S.C. 103(a) as being purportedly obvious over Berezin, US Patent No. 6,388,243, in view of Noguchi, US Patent No. 4,841,346. In addition, Claims 10 and 12-16 were rejected under 35 U.S.C. 103(a) as being purportedly obvious over Berezin in view of Noguchi and further in view of Fratin et al., US Patent No. 5,977,591. Applicant respectfully traverses these rejections.

With regard to independent claim 1, Applicants teach and claim a sensor having a transistor with a gate located partially over a source and partially over a drain. Applicants have amended claim 1 to reflect that the sensor includes a well region formed to below the source (or the drain in an alternate embodiment) such that a portion of the well region extends partially beneath the gate. Applicants further teach that the sensor has a material disposed between the well region and the drain (or the source in the alternate embodiment) that is defined by the separation of the source and drain beneath the gate, where the material has a predetermined length that is 20 percent longer than a process minimum, such as the process minimum gate

length of 0.35 microns. Applicants teach that by forming the well region such that only a portion of the well region extends below the gate, the well region does not contact the drain and, thus, increases the threshold of the gate (e.g., increasing "punch through" of channel well portion to the drain) to avoid soft resets of the gate. Applicants further teach that in one embodiment by adding an implant, such as a shallow boron implant, in the material to extend between the well region and the drain, the threshold of the gate is further increased and junction leakage is substantially controlled. Applicants also teach that in another embodiment by splitting the function of the gate so that the gate has an n-type region over the well region and a p-type region over the material, the threshold of the gate is further increased and junction leakage is substantially controlled. (See Application at pg. 6 line 14 - pg. 9 line 4; pg. 10 lines 14-21; Figs. 2, 3, and 5).

Berezin does not a sensor having a transistor with a gate located partially over a source and partially over a drain. In addition, neither Berezin nor Noguchi teach or suggest, alone or in combination, the Claim 1 limitations of *a well region formed beneath the source such that a portion of the well region extends partially beneath the gate* and *a material disposed between the well region and the drain beneath the gate, the material having a predetermined length* as taught and claimed by Applicants.

Accordingly, Applicants request that the Examiner withdraw the rejection to Claim 1.

Claims 2-17 depend from Claim 1 and should be deemed allowable for at least the same reasons as Claim 1. Accordingly, Applicants request that the Examiner remove the rejections to these claims.

V. Newly Added Claims

Applicants respectfully request consideration of newly added claims 50-58 that further distinguish applicants invention. In particular, Claims 50-54 are directed to a sensor that has, among other limitations, a transistor with a gate located partially over a source and partially over a drain formed in a substrate, where the sensor has a well region formed to contain one of the source and the drain such that a portion of the well region extends partially beneath the gate and an implant formed in the substrate to extend between the well region and the other of the source and the drain such that the implant increases a surface threshold of the transistor. Claims 55-58 are directed to a sensor that has, among other limitations, a transistor having a source, a drain, and a gate located partially over the source and partially over the drain, the gate having a p-type region and a n-type region, and a well region formed to contain one of the source and the drain and to extend partially beneath the gate such that the well region extends a length of one of the n-type and the p-type gate regions.

None of the references cited by the Examiner, alone or in combination, discloses a sensor having the limitations recited in Claims 50-58.

CONCLUSION

In view of the above amendments and remarks, Applicant submits that all claims now pending are clearly allowable over the cited prior art, and respectfully requests early and favorable notification to that effect. If the Examiner believes that a conference would be of

value in expediting the prosecution of this application, the Examiner is invited to telephone the undersigned counsel to arrange for such a conference.

Respectfully submitted,

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APPENDIX A
CLEAN VERSION WITHOUT MARKINGS TO SHOW CHANGES MADE IN SPECIFICATION

Please substitute the paragraph beginning on page 7, line 4 with the following paragraph:

B'

The transistor 104 of sensor 100 further includes a material in the space defined by the separation of the source 106 from the drain 110 beneath the gate 108. In an example implementation of the transistor 104, the length 206 of the material is at least 20 percent longer than a process minimum. For example, the process minimum gate length for a conventional 3.3 volt logic process range is approximately .35 microns. The recommended minimum gate length to avoid exaggerated short channel effects would be approximately 0.4 microns. While increasing the length 206 by approximately 20 percent of the process minimum increases the potential required to deplete the reset channel. In one embodiment, the gate 108 may have a predetermined length that is approximately twice the process minimum (e.g., 0.35 micorons) based on the material length 206. But, the increase in potential required to deplete the reset channel. But, the increase in potential required to deplete the reset channel significantly decreases the likelihood of a soft reset during a read operation (i.e. subthreshold leakage does not degrade low light operation) and promotes the proper functioning of the various forms of tapered reset. An additional result of increasing the length of the gate 108 is that the doping of the gate 108, source 106, drain 110, and associated channel may be decreased.

Please substitute the paragraph beginning on page 8, line 13 with the following paragraph:

In FIG. 3, a cross sectional view of an exemplary implementation of the sensor 300 of FIG. 1 is illustrated. The FET transistor 302 has a gate 304, a source 306, and a drain 308. The drain 308 of the transistor 302 is connected to the deep implant 316 of photo-detector 310. The gate 304 has a n-type region 312, a p-type region 314, and a dielectric insulator 316. The source 306 includes a p-type well 318 located in a substrate 320. In this implementation, material is located between the p-type well 318 of the source 306 and the drain 308. The length 322 of the material is defined by the separation of the source 306 from the drain 308 beneath the gate 304. The length 322 of the material is preferably at least 20 percent longer than the process minimum. As a result, the gate 108 may have a predetermined length that is approximately twice the process minimum.

B2

APPENDIX B
CLEAN VERSION WITHOUT MARKINGS TO SHOW CHANGES MADE IN CLAIMS

Please substitute claims 1-2, 4-6, 11, 13, and 15 and add claims 50-58 as follows:

1. (Amended) A sensor having a transistor with a gate located partially over a source and partially over a drain, comprising:

a well region formed beneath the source such that a portion of the well region extends partially beneath the gate;

B3

a material disposed between the well region and the drain beneath the gate, the material having a predetermined length; and

a detection device coupled to the drain by a signal path, wherein the material allows the detection device to be reset to a predetermined state.

2. (Amended) The sensor of claim 1, further including an implant in the material that increases a surface threshold of the transistor.

4. (Amended) The sensor of claim 2, wherein the implant is formed to extend between the well region and the drain.

B4

5. (Amended) The sensor of claim 3, wherein the implant has a dopant concentration that is less than the well region.

6. (Amended) The sensor of claim 2, wherein the implant is a shallow boron implant.

B5

11. (Amended) The sensor of claim 10, wherein the gate has a predetermined length that is approximately two times a process minimum.

B6

13. (Amended) The sensor of claim 12, wherein the material corresponds to a portion of a p-type substrate that is in proximity to the p-type region of the gate and the portion of the well region extends beneath the n-type region of the gate.

B7

15. (Amended) The sensor of claim 10, including an implant region located in the drain extending under the p-type region of the gate such that the drain is not in direct contact with the gate.

B8

50. (New) A sensor having a transistor with a gate located partially over a source and partially over a drain formed in a substrate, comprising:

a well region formed to contain one of the source and the drain such that a portion of the well region extends partially beneath the gate;

an implant formed in the substrate to extend between the well region and the other of the source and the drain such that the implant increases a surface threshold of the transistor; and

a detection device coupled to the drain by a signal path, wherein the implant allows the detection device to be reset to a predetermined state when a voltage that is greater than or equal to the surface threshold of the transistor is present on the gate.

51. (New) The sensor of claim 50, wherein the surface threshold of the transistor is increased to at least 0.8 volts.

52. (New) The sensor of claim 50, wherein the gate has a predetermined length and the implant extends approximately a half of the predetermined length of the gate.

53. (New) The sensor of claim 52, wherein the predetermined length of the gate is at least 20 percent greater than a process minimum.

54. (New) The sensor of claim 52, wherein the predetermined length of the gate is approximately two times a process minimum.

55. (New) A sensor, comprising:

a transistor having a source, a drain, and a gate located partially over the source and partially over the drain, the gate having a p-type region and a n-type region;

a well region formed to contain one of the source and the drain and to extend partially beneath the gate such that the well region extends a length of one of the n-type and the p-type gate regions; and

B3 concl'd

a detection device coupled to the drain by a signal path.

56. (New) The sensor of claim 55, wherein the gate has a predetermined length that is approximately two times a process minimum.

57. (New) The sensor of claim 55, wherein the well region is a p-type material and the well region extends the length of the n-type gate region.

58. (New) The sensor of claim 57, further comprising an implant region located in the drain extending under the p-type region of the gate such that the drain is not in direct contact with the gate.